

Amendments to the Specification:

Please replace the text beginning at page 4, line 10, and ending at the bottom of page 6, line 23, as follows:

Further details of a presently preferred ManArray core, architecture, and instructions for use in conjunction with the present invention are found in

U.S. Patent Application Serial No. 08/885,310 filed June 30, 1997, now U.S. Patent No. 6,023,753,

U.S. Patent Application Serial No. 08/949,122 filed October 10, 1997, now U.S. Patent No. 6,167,502.

U.S. Patent Application Serial No. 09/169,255 filed October 9, 1998, now U.S. Patent No. 6,343,356.

U.S. Patent Application Serial No. 09/169,256 filed October 9, 1998, now U. S. Patent No. 6,167,501.

U.S. Patent Application Serial No. 09/169,072, filed October 9, 1998, now U.S. Patent No. 6,219,776.

U.S. Patent Application Serial No. 09/187,539 filed November 6, 1998, now U.S. Patent No. 6,151,668.

U.S. Patent Application Serial No. 09/205,588 filed December 4, 1998, now U.S. Patent No. 6,173,389.

U.S. Patent Application Serial No. 09/215,081 filed December 18, 1998, now U.S. Patent No. 6,101,592.

U.S. Patent Application Serial No. 09/228,374 filed January 12, 1999 now U.S. Patent No. 6,216,223, and entitled "~~Methods and Apparatus to Dynamically Reconfigure the Instruction Pipeline of an Indirect Very Long Instruction Word Scalable Processor~~",

U.S. Patent Application Serial No. 09/238,446 filed January 28, 1999, now U.S. Patent No. 6,366,999,

U.S. Patent Application Serial No. 09/267,570 filed March 12, 1999, now U.S. Patent No. 6,446,190,

U.S. Patent Application Serial No. 09/337,839 filed June 22, 1999,

U.S. Patent Application Serial No. 09/350,191 filed July 9, 1999, now U.S. Patent No. 6,356,994,

U.S. Patent Application Serial No. 09/422,015 filed October 21, 1999 entitled "~~Methods and Apparatus for Abbreviated Instruction and Configurable Processor Architecture~~", now U.S. Patent No. 6,408,382,

U.S. Patent Application Serial No. 09/432,705 filed November 2, 1999 entitled "Methods and Apparatus for Improved Motion Estimation for Video Encoding",

U.S. Patent Application Serial No. 09/471,217 filed December 23, 1999 entitled "Methods and Apparatus for Providing Data Transfer Control",

U.S. Patent Application Serial No. 09/472,372 filed December 23, 1999 entitled "~~Methods and Apparatus for Providing Direct Memory Access Control~~", now U.S. Patent No. 6,256,683,

U.S. Patent Application Serial No. 09/596,103 entitled "~~Methods and Apparatus for Data Dependent Address Operations and Efficient Variable Length Code Decoding in a VLIW Processor~~" filed June 16, 2000, now U.S. Patent No. 6,397,324,

U.S. Patent Application Serial No. 09/598,567 entitled "Methods and Apparatus for Improved Efficiency in Pipeline Simulation and Emulation" filed June 21, 2000,

U.S. Patent Application Serial No. 09/598,564 ~~entitled "Methods and Apparatus for Initiating and Resynchronizing Multi-Cycle SIMD Instructions"~~ filed June 21, 2000, now U.S. Patent No. 6,622,234,

U.S. Patent Application Serial No. 09/598,558 entitled "Methods and Apparatus for Providing Manifold Array (ManArray) Program Context Switch with Array Reconfiguration Control" filed June 21, 2000, and

U.S. Patent Application Serial No. 09/598,084 ~~entitled "Methods and Apparatus for Establishing Port Priority Functions in a VLIW Processor"~~ filed June 21, 2000, now U.S. Patent No. 6,654,870, and

U.S. Patent Application Serial No. 09/598,566 entitled "Methods and Apparatus for Generalized Event Detection and Action Specification in A Processor" filed June 21, 2000, as well as,

Provisional Application Serial No. 60/113,637 entitled "Methods and Apparatus for Providing Direct Memory Access (DMA) Engine" filed December 23, 1998,

Provisional Application Serial No. 60/113,555 entitled "Methods and Apparatus Providing Transfer Control" filed December 23, 1998,

Provisional Application Serial No. 60/139,946 entitled "Methods and Apparatus for Data Dependent Address Operations and Efficient Variable Length Code Decoding in a VLIW Processor" filed June 18, 1999,

Provisional Application Serial No. 60/140,245 entitled "Methods and Apparatus for Generalized Event Detection and Action Specification in a Processor" filed June 21, 1999,

Provisional Application Serial No. 60/140,163 entitled "Methods and Apparatus for Improved Efficiency in Pipeline Simulation and Emulation" filed June 21, 1999,

Provisional Application Serial No. 60/140,162 entitled "Methods and Apparatus for Initiating and Re-Synchronizing Multi-Cycle SIMD Instructions" filed June 21, 1999,

Provisional Application Serial No. 60/140,244 entitled "Methods and Apparatus for Providing One-By-One Manifold Array (1x1 ManArray) Program Context Control" filed June 21, 1999,

Provisional Application Serial No. 60/140,325 entitled "Methods and Apparatus for Establishing Port Priority Function in a VLIW Processor" filed June 21, 1999,

Provisional Application Serial No. 60/140,425 entitled "Methods and Apparatus for Parallel Processing Utilizing a Manifold Array (ManArray) Architecture and Instruction Syntax" filed June 22, 1999,

Provisional Application Serial No. 60/165,337 entitled "Efficient Cosine Transform Implementations on the ManArray Architecture" filed November 12, 1999, and

Provisional Application Serial No. 60/171,911 entitled "Methods and Apparatus for DMA Loading of Very Long Instruction Word Memory" filed December 23, 1999,

Provisional Application Serial No. 60/184,668 entitled "Methods and Apparatus for Providing Bit-Reversal and Multicast Functions Utilizing DMA Controller" filed February 24, 2000,

Provisional Application Serial No. 60/184,529 entitled "Methods and Apparatus for Scalable Array Processor Interrupt Detection and Response" filed February 24, 2000,

Provisional Application Serial No. 60/184,560 entitled "Methods and Apparatus for Flexible Strength Coprocessing Interface" filed February 24, 2000,

Provisional Application Serial No. 60/203,629 entitled "Methods and Apparatus for Power Control in a Scalable Array of Processor Elements" filed May 12, 2000, respectively, all of which are assigned to the assignee of the present invention and incorporated by reference herein in their entirety.